MINSOO KIM

minsook@nvidia.com | Austin, TX 78717 | (858) 361-6821 | minsookim.me | linkedin.com/in/minsoo-kim-4289abb8

SUMMARY

I am currently employed as a Senior CAD Engineer at NVIDIA Corporation, where my primary focus is on standard cell physical design automation. Prior to completing my PhD, I gained experience as a physical design engineer in the Design Technology team at Samsung Foundry. I actively contributed to the development of advanced physical design methodologies for cutting-edge technology process nodes. My professional and research interests are centered around standard cell layout automation, technology-aware physical design methodology, design-technology co-optimization (DTCO), and leveraging machine learning for prediction and optimization in physical design. These areas of expertise drive my current work and represent my future aspirations in the field.

EDUCATION

UNIVERSITY OF CALIFORNIA SAN DIEGO (UCSD)
Ph.D., Electrical and Computer Engineering (GPA: 4.0/4.0) June 2023
- Advised by Prof. Andrew B. Kahng

KOREA ADVANCED INSTITUTE OF SCIENCE AND TECHNOLOGY (KAIST)
M.S., Electrical Engineering (GPA: 3.1/4.0) February 2013
- Advised by Prof. Chong-Min Kyung

YONSEI UNIVERSITY
B.S., Electrical Engineering (GPA: 3.7/4.0) February 2011

EXPERIENCE

NVIDIA CORP., Austin, TX, USA **06/2022-Present**
Senior CAD Engineer, Physical Design
- Developing and enhancing automated layout generation of standard cells in new process technologies

UNIVERSITY OF CALIFORNIA SAN DIEGO, San Diego, CA, USA **09/2017-06/2022**
Graduate Student Researcher
- Developed DTCO methodology for PPAC evaluations at an early stage of technology development (w/ IBM, Samsung)
- Developed machine learning (ML)-assisted pathfinding for advanced nodes (w/ Qualcomm)
- Developed technology-aware leakage optimization and power stapling methodology for advanced nodes (w/ Samsung)
- Developed top-level clock tree synthesis (CTS) optimization for memory-dominant system-on-chip (w/ NXP)
- Participated in the open-sourcing research project (OpenROAD) (https://theopenroadproject.org) supported by DARPA
- Experienced with 7, 12, 14, 16, 28, 45, 65 and 130nm technologies from multiple academia/industry PDKs

QUALCOMM TECHNOLOGIES, INC., San Diego, CA, USA **06/2021-09/2021**
Interim Engineering Intern (Remote)
- Enabled routability and IR drop analysis at 4nm technology

CADENCE DESIGN SYSTEMS, INC., Austin, TX, USA **06/2020-09/2020**
Software Intern (Remote)
- Developed a buffering methodology for detailed balancing of clock trees in clock tree synthesis stage (Innovus)

SAMSUNG ELECTRONICS CO. LTD., Hwaseong, Gyeonggi, South Korea **02/2013-07/2017**
Physical Design Engineer
- Developed physical design methodologies for Samsung 7, 8, 10, 14, 28nm technology nodes
- Developed reference flows and technology files of ICC and ICC2 for Samsung 10, 14, 28nm technology nodes
- Enabled new design rules in P&R tools for 10, 14, 28nm technology nodes
- Technical support for Samsung foundry customers (Qualcomm, NVIDIA, AMD, ST Microelectronics)
- Worked with EDA vendors (Cadence, Synopsys and Mentor Graphics) for tool development at advanced technologies
- Experienced with multiple SoC projects for design verification (including STA, DRC, LVS)
- Participated in physical design and tape-out of the world-first Samsung 10nm SoC project

SKILLS

- VLSI physical design from RTL to GDS
- Design and technology co-optimization (DTCO)
- Machine learning in physical design

- Physical design and verification (signoff) experiences in industry and academia
- **EDA Tool**: DC, ICC, ICC2, FC, Genus, Innovus, Primetime, Tempus, Calibre (DRC/LVS/PEX), ICV, Redhawk(-SC), Virtuoso, Voltus, StarRC, Liberate, SiliconSmart, HSPICE
- **Programming Language**: Verilog HDL, **TCL**, C/**C++, Python, Perl**

PUBLICATIONS

(*All papers with Prof. Andrew B. Kahng, have authors listed in alphabetical order)**

Journal

- [J3] S. Choi, J. Jung, A. B. Kahng, **Minsoo Kim**, C.-H. Park, B. Pramanik and D. Yoon, "**PROBE3.0: A Systematic Framework for Design-Technology Pathfinding with Improved Design Enablement**", In revision to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.
- [J2] A. B. Kahng, **Minsoo Kim**, S. Kim and M. Woo, "**RosettaStone: Connecting the Past, Present and Future of Physical Design Research**", *IEEE Design & Test* 39(5) (2022), pp. 70-78.
- [J1] C.-K. Cheng, A. B. Kahng, H. Kim, **Minsoo Kim**, D. Lee, D. Park and M. Woo **"PROBE2.0: A Systematic Framework for Routability Assessment from Technology to Design in Advanced Nodes"**, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2022), pp. 1495-1508.

Conference

- [C12] C.-T. Ho, A. Chandra, D. Guan, A. Ho, **Minsoo Kim**, Y. Li and H. Ren, "**Novel Transformer Model Based Clustering Method for Standard Cell Design Automation**", *Proc. ACM/IEEE International Symposium on Physical Design*, 2024, to appear. **(Nominated for Best Paper awards)**
- [C11] C.-T. Ho, A. Ho, M. Fojtik, **Minsoo Kim**, S. Wei, Y. Li, B. Khailany and H. Ren, "**NVCell 2: Routability-Driven Standard Cell Layout in Advanced Nodes with Lattice Graph Routability Model**", *Proc. ACM/IEEE International Symposium on Physical Design*, 2023, pp. 44-52.
- [C10] C.-K. Cheng, A. B. Kahng, I. Kang, **Minsoo Kim**, D. Lee, B. Lin, D. Park and M. Woo, "**CoRe-ECO: Concurrent Refinement of Detailed Place-and-Route for an Efficient ECO Automation**", *Proc. IEEE International Conference on Computer Design*, 2021, pp. 366-373.
- [C9] C. Chidambaram, A. B. Kahng, **Minsoo Kim**, G. Nallapati, S. C. Song and M. Woo, **"A Novel Framework for DTCO: Fast and Automatic Routability Assessment with Machine Learning for Sub-3nm Technology Options"**, *Proc. IEEE Symposium on VLSI Technology*, 2021, pp. 1-2.
- [C8] H. Fatemi, A. B. Kahng, **Minsoo Kim** and J. Pineda de Gyvez **"Optimal Bounded-Skew Steiner Trees to Minimize Maximum k-Active Dynamic Power"**, *Proc. ACM/IEEE International Workshop on System-Level Interconnect Problems and Pathfinding*, 2020, pp. 1-8.
- [C7] A. Rovinski, T. Ajayi, **Minsoo Kim**, G. Wang and M. Saligane, **"Bridging Academic Open-Source EDA to Real-World Usability"**, *Proc. ACM/IEEE International Conference on Computer-Aided Design*, 2020, pp. 1-7.
- [C6] V. A. Chhabria, A. B. Kahng, **Minsoo Kim**, U. Mallappa, S. S. Sapatnekar and B. Xu, **"Template-based PDN Synthesis in Floorplan and Placement Using Classifier and CNN Techniques"**, *Proc. ACM/IEEE Asia and South Pacific Design Automation Conference*, 2020, pp. 44-49.
- [C5] T. Ajayi, V. A. Chhabria, M. Fogaça, S. Hashemi, A. Hosny, A. B. Kahng, **Minsoo Kim**, J. Lee, U. Mallappa, M. Neseem, G. Pradipta, S. Reda, M. Saligane, S. S. Sapatnekar, C. Sechen, M. Shalan, W. Swartz, L. Wang, Z. Wang, M. Woo and B. Xu, **"Toward an Open-Source Digital Flow: First Learnings from the OpenROAD Project"**, *Proc. ACM/IEEE Design Automation Conference*, 2019, pp. 76:1-76:4.
- [C4] T. Ajayi, D. Blaauw, T.-B. Chan, C.-K. Cheng, V. A. Chhabria, D. K. Choo, M. Coltella, S. Dobre, R. Dreslinski, M. Fogaça, S. Hashemi, A. Hosny, A. B. Kahng, **Minsoo Kim**, J. Li, Z. Liang, U. Mallappa, P. Penzes, G. Pradipta, S. Reda, A. Rovinski, K. Samadi, S. S. Sapatnekar, L. Saul, C. Sechen, V. Srinivas, W. Swartz, D. Sylvester, D. Urquhart, L. Wang, M. Woo and B. Xu, **"OpenROAD: Toward a Self- Driving, Open-Source Digital Layout Implementation Tool Chain"**, *Proc. Government Microcircuit Applications and Critical Technology Conference*, 2019, pp. 1105-1110.
- [C3] S. Heo, A. B. Kahng, **Minsoo Kim**, L. Wang and C. Yang **"Detailed Placement for IR Drop Mitigation by Power Staple Insertion in Sub-10nm"**, *Proc. ACM/IEEE Design, Automation and Test in Europe*, 2019, pp. 824-829.
- [C2] S. Heo, A. B. Kahng, **Minsoo Kim** and L. Wang, **"Diffusion Break-Aware Leakage Power Optimization and Detailed Placement in Sub-10nm VLSI"**, *Proc. ACM/IEEE Asia and South Pacific Design Automation Conference*, 2019, pp. 550-556. **(Nominated for Best Paper awards)**
- [C1] **Minsoo Kim**, C.-M. Kyung and K. Yi, **"An Energy Management Scheme for Solar-Powered Wireless Visual Sensor Networks Toward Uninterrupted Operations"**, *Proc. IEEE International SoC Design Conference*, 2013, pp. 23-26.